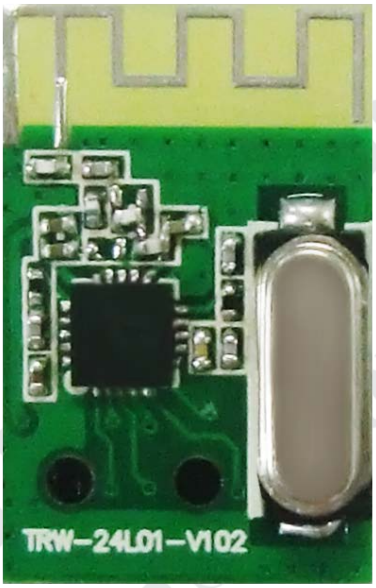
WENSHING®©

TRW-24L01 MODULE

2.4G ISM Transceiver



Version History

Version	Date	Changes
V1.00	August 15, 2013	1st. Edition

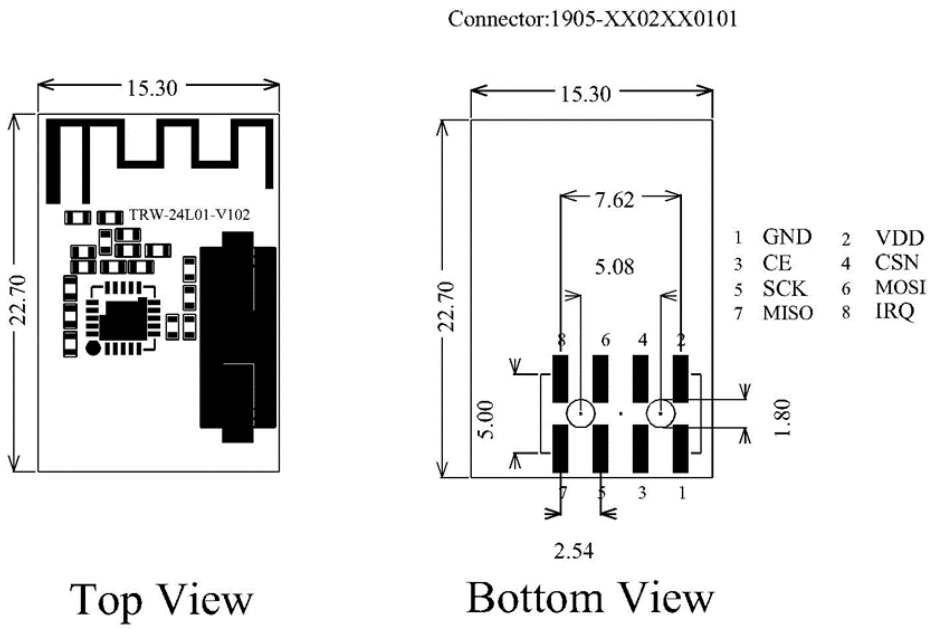
Key Features

- Worldwide 2.4GHz ISM band operation
- 250kbps, 1Mbps and 2Mbps on air datarates
- Ultra low power operation
- Programmable power:, -25, -15, -5, 0, 5 dBm
- 900nA in power down
- 26μA in standby-I
- RF CHIP Drop-in compatibility with nRF24L0
- Low cost
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™

Applications

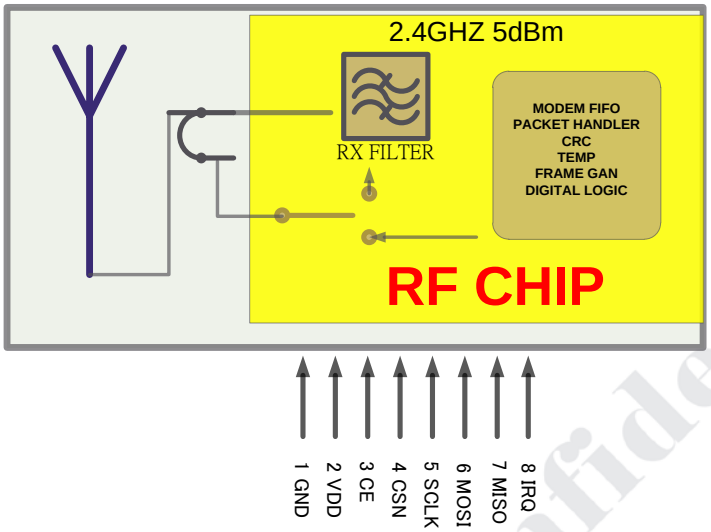
- Wireless PC Peripherals
- 3-in-1 desktop bundles
- Toys
- Sports watches and sensors
- Home and commercial automation
- Active RFID
- Mouse, keyboards and remotes
- Advanced Media center remote controls
- Game controllers
- RF remote controls for consumer electronics
- Ultra low power sensor networks
- Asset tracking systems

Size View



Block Diagram

TRW-24L01 Function Block Diagram



1 Pin Function

Pin	Name	I/O	Description
1	GND	GND	Ground.
2	VCC	Input	+1.8 to +3.6 V Supply Voltage Input to Internal Regulators
3	CE	Digital Input	Chip Enable Activates RX or TX mode
4	CSN	Digital Input	SPI Chip Select
5	SCK	Digital Input	SPI Clock
6	MOSI	Digital Input	SPI Slave Data Input
7	MISO	Digital Output	SPI Slave Data Output with tri-state option
8	IRQ	Digital Output	Mask able interrupt pin. Active low

2 Hardware Specification

2.1 Specification

Conditions: VDD =VCC= +3.3V, VSS = 0V, TA =25ºC

Parameter	Description	Min	Typ	Max	Unit
VDD	Supply Voltage Range	1.9	3.3	3.6V	V
IPD	Power down current		9		uA
ISTBY	Standby current		47		uA
FREQ	Operating frequency	2400		2484	MHz
FSPACE	Channel spacing		1		MHz
FXTAL	Crystal frequency		16		MHz
TOLXTAL	Crystal tolerance	-60		60	Ppm
FD250K	Frequency deviation @250Kbps			1000	kHz
FD1M	Frequency deviation @1Mbps			1100	kHz
FD2M	Frequency deviation @2Mbps			2500	kHz
T_TRX	Standby to TX/RX time		130		us
IDC_TXMID	TX DC current, 0dBm output power		20.5		mA
IDC_TXMIN	TX DC current, minimum output power		10.8		mA
IDC_RX	RX DC current consumption		26.6		mA
PMAX	Output power at maximum power		5		dBm
PMIN	Output power at minimum power		-40		dBm
PACC	Power accuracy		2		dB
SENS_250	Sensitivity <0.1% BER 250kbps		-92		dBm
SENS_1M	Sensitivity <0.1% BER 1Mbps		-90		dBm
SENS_2M	Sensitivity <0.1% BER 2Mbps		-88		dBm
CI_250	Co-channel rejection C/I @ 250kbps		3		dB
CI_1M	Co-channel rejection C/I @ 1Mbps		5		dB
CI_2M	Co-channel rejection C/I @ 2Mbps		8		dB
BLK1M_1	1Mbps C/I in-band block 1MHz offset		-2		dB
BLK1M_2	1Mbps C/I in-band block 2MHz offset		-21		dB
BLK1M_3	1Mbps C/I in-band block 3MHz offset		-24		dB
BLK2M_2	2Mbps C/I in-band block 2MHz offset		-21		dB
BLK2M_4	2Mbps C/I in-band block 4MHz offset		-22		dB
BLK2M_6	2Mbps C/I in-band block 6MHz offset		-35		dB

3 CONTROL STATES

3.1 STATE DIAGRAM

TRW-24L01 can be set up as a primary transmitter (PTX) or a primary receiver (PRX). A transmission pair must be set up as a PTX and a PRX, i.e. 2 PTXs cannot communicate with each other, and neither can two PRXs. PTX/PRX is setup by the RX_ON bit. Setting 0 makes device a PTX, and setting 1 makes device a PRX.

Figure 3 shows the typical state diagram of TRW-24L01 with auto-acknowledgement (auto-ACK) feature disabled. Operation states are fully controlled by the MCU through the power **VDD**, hardwire pin **CE**, and register bits PWR_ON and RX_ON.

When auto-ACK is enabled, PTX automatically switches to RX mode to receive the ACK packet, switching back to TX for retransmission if necessary; PRX automatically switches to TX mode to send the ACK packet. Figure 4 shows the PTX state diagram in auto-ACK mode, and Figure 5 shows the PRX state diagram in auto-ACK mode.

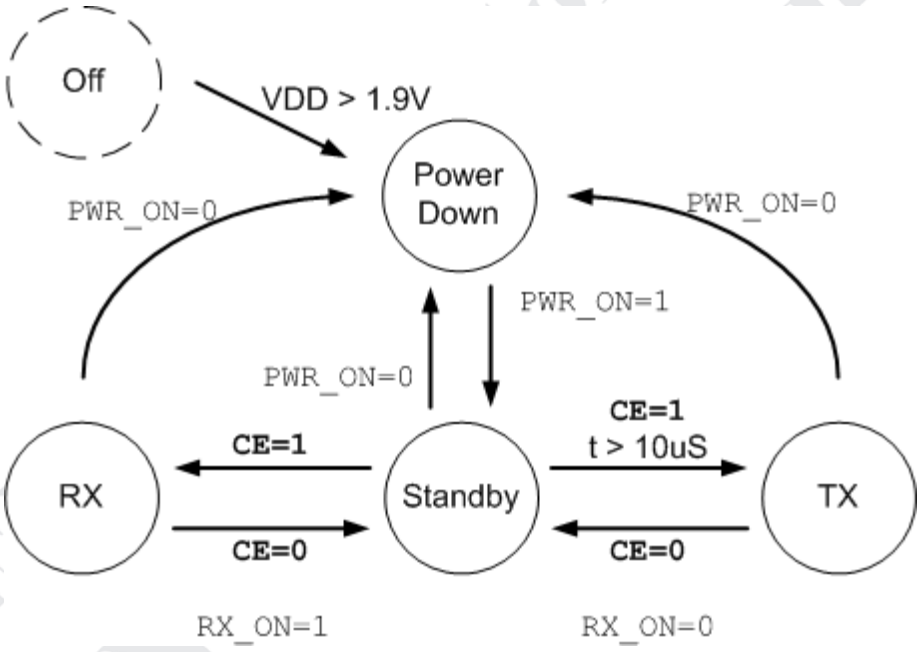


Figure 3: TRW-24L01 State Diagram

3.1.1 POWER-ON RESET

When power is applied to **VDD** and is over 1.9V threshold, TRW-24L01 will run power-on reset. Once power-on reset is completed, the device will be in power-down mode.

3.1.2 POWER-DOWN MODE

In power-down mode, TRW-24L01 is in deep-sleep and only the SPI interface is active. TRW-24L01 is in power-down mode when PWR_ON is set to 0.

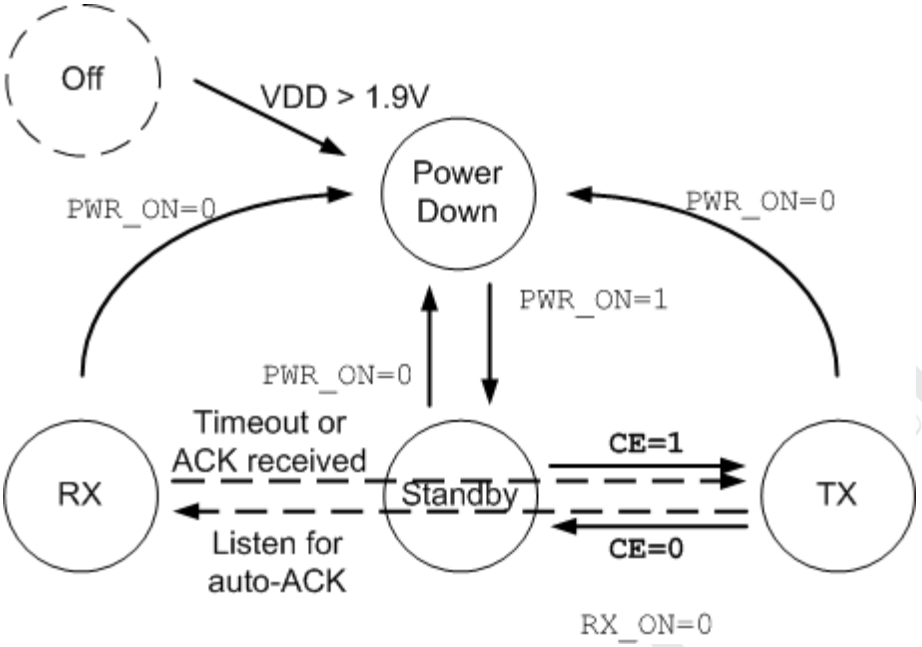


Figure 5: PTX with auto-ACK

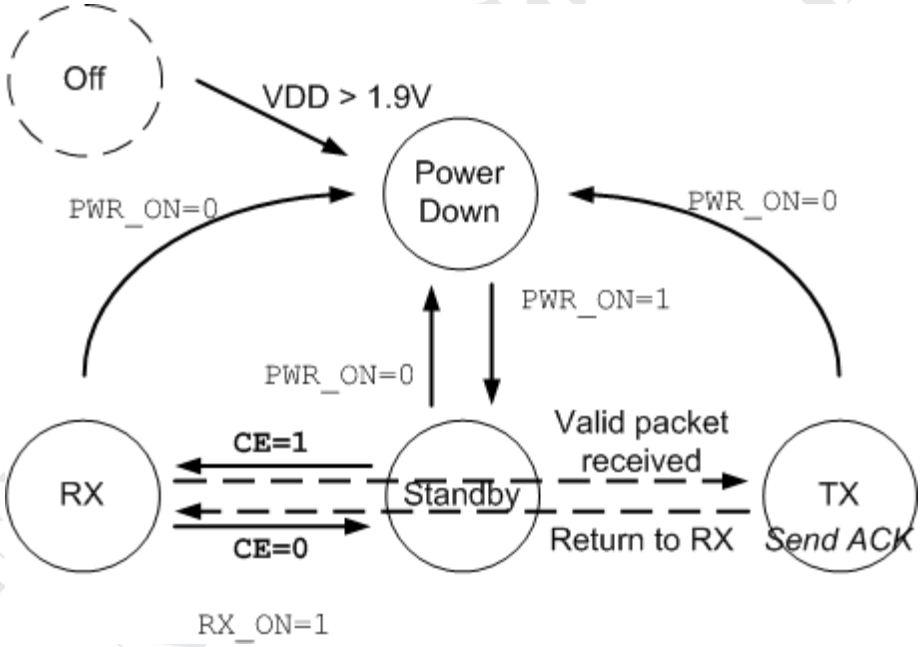


Figure 4: PRX with auto ACK

The device enters power-down mode whenever PWR_ON is set to zero.

3.1.3 STANDBY MODE

Setting PWR_ON bit to “1” will activate device to standby mode (while **CE** remains 0). In standby mode, the crystal oscillator is active, and the device is ready to quickly enter TX or RX mode.

3.1.4 TX MODE

TRW-24L01 transmits packets in TX mode. To operate in TX mode, the device needs to be set up as a PTX (RX_ON=0), standby mode (PWR_ON=1), and a payload(s) in FIFO. There are two modes of TX: pulsed (single packet mode) and continuous mode. A **CE** high pulse of at least 10 us triggers a single packet to be sent. Keeping **CE** high will set the device to continuous TX mode, which will send out all packets in FIFO. After FIFO is emptied, the device will power-off radio and digital baseband to save current, but the device will commence transmission as soon as a new payload enters FIFO.

When auto-ACK feature is enabled, a PRX device automatically enters TX mode to send back an ACK packet after a valid packet is received from a PTX.

3.1.5 RX MODE

TRW-24L01 receives packets in RX mode. The device needs to be set up as a PRX (RX_ON=1) and in standby mode (PWR_ON=1). Pulling **CE** pin high sets the device to RX mode and will continue listening for packets as long as **CE** is held high. Payloads of valid packets will be placed into the RX FIFO.

When auto-ACK feature is enabled, a PTX device automatically enters RX mode after transmission to listen for an ACK packet from the PRX.

3.2 RADIO SETUP

TRW-24L01 supports 250kbps, 1Mbps, and 2 Mbps air bit rate. The choice of which bit rate to use depends on range, current consumption, and data rate needed. Lower bit rate has longer range, while higher bit rate has lower current consumption and reduced probability of in-air collision. Air rate is set by the SETUP_RF register.

The channel may be set in 1 MHz increment from 2400 MHz to 2484 MHz. Although it is possible to set the channel frequency higher than 2484 MHz, it is not recommended for this may violate regional regulations. For 250kbps and 1Mbps operation, the channel may be set in 1 MHz increment; for 2Mbps operation, the channel spacing should be 2 MHz or more. Channel selection is set by the RF_CH register.

In addition to the device address, the bit rate and channel frequency need to be set the same for the radios to communicate with each other.

3.3 RSSI RECORDER

TRW-24L01 features an advanced RSSI block and control, allowing the receiver host to collect detailed information of the current RX channel. There are two decision thresholds that can be individually set. An RSSI recorder generates a log of the channel traffic. With two decision thresholds, the host can separate the receiving signal into three ranges: low, medium, and high. The RSSI recorder consists of two 8-bit shift registers corresponding to the two thresholds, and it keeps track of the RSSI readings for the past 8 time slots. A single time slot is 128 us. This advanced RSSI

scheme can be useful in detecting complex channel behaviors such as fading, interference, and may assist MCU in channel selection.

The RSSI enable setting and RSSI readout are in the RSSI register setting. The RSSI threshold and recorder are in address 0x18. Figure 6 shows the basic concept of the RSSI recorder scheme. At read point 1, [RSSI1, RSSI2] readout will be [0,0], RSSIREC1 readout will be 0xF8 and RSSIREC2 readout will be 0x60; at read point 2, [RSSI1, RSSI2] will read [0,1], RSSIREC1 will read 0x0F and RSSIREC2 will read 0x08.

TRW-24L01 also has a unique identifier encoded in [RSSIREC2, RSSIREC1] and can be read right after POR. The 16-bit unique ID for TRW-24L01 is 0x7241.

To save current, the RSSI is set to be off by default. To turn on the RSSI, enable bit 4 of the RSSI register. The two decision thresholds are also indicated at bit 0 and bit 1 of the RSSI register.

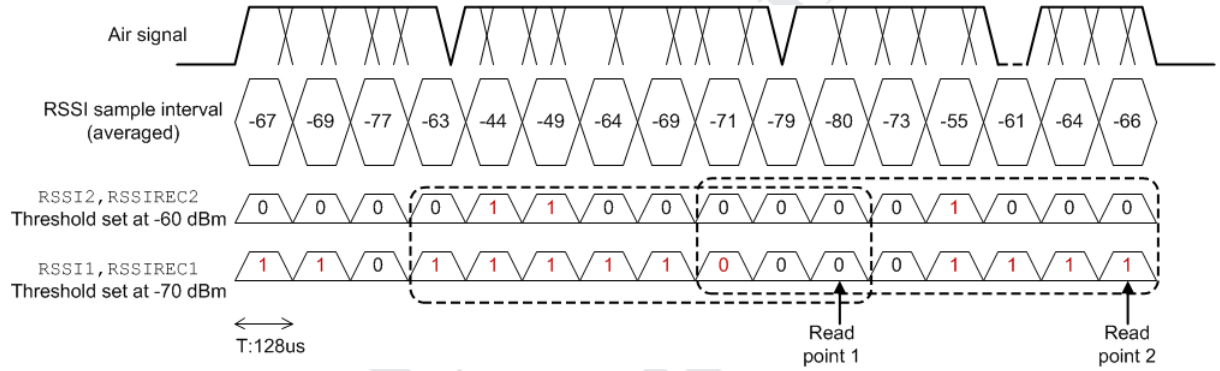


Figure 6: RSSI recorder scheme

4 PACKET INFORMATION

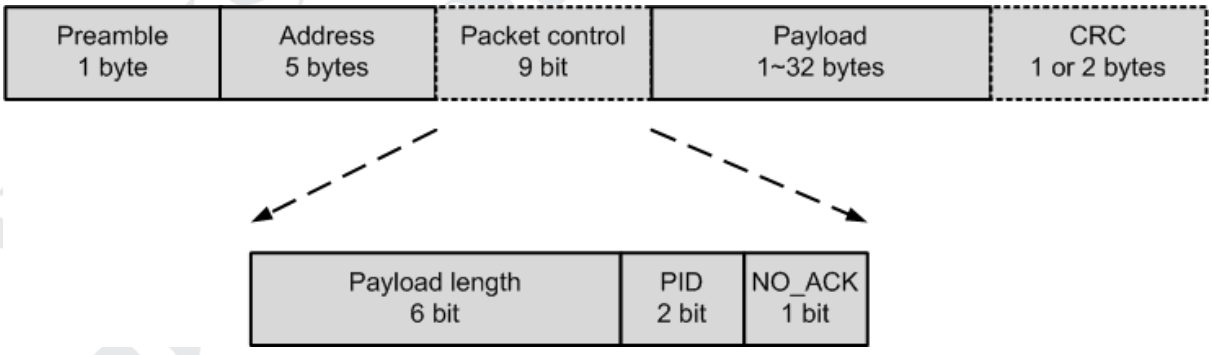


Figure 7: Packet Format

The packet consists of 5 portions: preamble, address, packet control, payload, and CRC. The preamble, address, and payload are required fields; packet control and CRC are optional fields, depending on settings.

4.1 PACKET FORMAT

4.1.1 PREAMBLE

The preamble is a one-byte alternating sequence of 01010101 or 10101010, depending on the first bit in the address. If the first address bit is 1 the preamble will be set to 10101010; if the first address bit is 0, the preamble is set to 01010101.

4.1.2 ADDRESS

This field holds the address of the receiver.

Addresses with only one or two transitions (e.g. 0x000005FFFF or 0x00FF000000) or as a continuation of the preamble (010101…) are not recommended for they may increase the packet error rate.

4.1.3 PACKET CONTROL

The packet control field consists of 9 bits, containing a 6-bit payload length field, a 2-bit packet identity (PID) field, and a one-bit NO_ACK flag.

The payload length is used when dynamic payload length feature is enabled. It specifies payload length in bytes, which can range from 1 to 32. Values higher than 32 are ignored.

The PID field is used to detect whether the packet is new or retransmitted. This field prevents the PRX from delivering the same payload more than once to the RX host MCU. The PID is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields are used together by the PRX to determine whether the received packet is retransmitted or new.

The NO_ACK flag is used when the auto-ACK feature is enabled. Setting the flag high tells the receiver that this packet does not need to be auto acknowledged. This flag is set on the PTX by using the command W_TX_PLOAD_NOACK, instead of W_TX_PLOAD, to write the TX payload. To use this function requires enabling the EN_DYN_ACK bit in the FEATURE register. When this option is used to transmit, the PTX goes directly to standby mode after transmitting the packet, and the PRX will not transmit an ACK packet after the packet is received.

4.1.4 PAYLOAD

The payload can be 1 to 32 bytes wide. The payload can be set either static or dynamic in length, defined by the packet control field. The default setup is static payload length. The static payload length is set by the RX_PW_Px register on the receiver side. Payload length on the transmitter side is set by the number of bytes placed in the TX_FIFO and must be equal to the value set in the RX_PW_Px register on the receiver side.

Dynamic payload length enables the transmitter to send packets of variable length to the receiver. The receiver can decode the payload length automatically from the control field value. The MCU can read the received payload length by using R_RX_PL_WID command.

To enable dynamic payload, set the EN_DPL bit in the FEATURE register to 1. In RX mode, the DYNPD register must be set. A PTX that transmits to a PRX with dynamic

payload enabled must have the DPL_P0 bit in DYNPD set.

4.1.5 CYCLIC REDUNDANCY CHECK (CRC)

The CRC is an error detection mechanism in the packet. It can be set to 1 or 2 bytes and is calculated over the address, packet control field, and payload.

The polynomial for 1-byte CRC is $X_8 + X_2 + X + 1$, with an initial value of 0xFF.

The polynomial for 2-byte CRC is $X_{16} + X_{12} + X_5 + 1$, with an initial value of 0xFFFF.

The CRCC bit in the CFG_TOP register sets the CRC length, and EN_CRC controls whether CRC is used. The CRC is a mandatory field for packets with auto-ACK or dynamic payload length enabled, and will override the EN_CRC bit setting. If CRC is enabled, packets will be dropped if CRC fails.

4.2 PACKET HANDLING

In TX mode, the PHY engine fetches a payload from TX FIFO, assembles the payload into a packet and transmits the packet in a short burst. After transmission, if the PTX packet has the NO_ACK flag set, the device sets TX_DS to 1 and gives an active low interrupt IRQ to MCU. If the PTX packet is an auto-ACK one, the PTX needs to receive an ACK from the PRX and then asserts the TX_DS IRQ.

The receiver continuously listens to the air channel for radio signal, and once it is synchronized to a likely signal, the PHY engine will validate the address and CRC of the possible packet. If a valid packet is detected and is a new one, the PHY engine writes the payload to RX FIFO, sets RX_DR to 1 and gives an active low interrupt IRQ to MCU.

When auto-acknowledge is enabled (EN_AA=1), the PTX will enter RX mode after transmission to wait for an ACK packet. If an ACK is not received within delay set by ARD[3:0], the PTX re-transmits the original packet and enters RX mode to wait for ACK. The above action is repeated until an ACK packet is received or the number of re-transmission exceeds a threshold set by ARC[3:0]. If the latter threshold is met, the PTX will set MAX_RT to 1 and give an active low interrupt IRQ to MCU. Two packet loss counters (ARC_CNT and PLOS_CNT) are incremented each time a packet is lost. The ARC_CNT counts the number of retransmissions for the current transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. Initiating a new transmission resets the ARC_CNT. Writing to the RF_CH register resets the PLOS_CNT. The ARC_CNT and the PLOS_CNT are in the OBSERVE_TX register. They may be used as an indicator of overall channel quality.

The PTX device will retransmit if its RX FIFO is full but receives an ACK packet with payload. As an alternative for the PTX to auto retransmit, it is possible to manually set the device to retransmit a packet a number of times. This is done by the REUSE_TX_PL command.

When auto-ACK is enabled, it is possible for the PRX to send a payload along with the ACK packet. To use this feature, the EN_ACK_PAY bit in the FEATURE register needs to be set. In addition, the dynamic payload function also needs to be set. The MCU at the PRX needs to upload the payload to the PRX's TX FIFO by using the W_ACK_PAYLOAD command. Payloads pending in the TX FIFO (of the PRX) will be sent after a new packet is received from PTX. Up to three payloads may be pending in the TX FIFO (of the PRX) at the same time.

5 DATA AND CONTROL INTERFACE

5.1 TX AND RX FIFO

TRW-24L01 has three levels of FIFO for the transmitter, and three levels of FIFO for receiver. Each FIFO level is 32 bytes in length. The TX FIFO is used to store payloads that are to be transmitted, and the RX FIFO is used to store the received payloads that have not been downloaded by the host MCU. Up to three payloads may be stored in a TX FIFO, and up to three payloads may be stored in an RX FIFO. The RX FIFO will also record which data pipe the payload comes from. Data pipe information is in the STATUS register and is read out from MISO during every SPI command. Successful transmission of a payload will clear a slot in the TX FIFO, and a reading from RX FIFO will clear an RX payload slot. Both FIFOs are accessed through the SPI using dedicated commands. Data access to the two FIFOs, as the name suggests, follows the first-in first-out principle.

In a PRX device, the TX FIFO can store payloads of ACK packets for up to three different PTX devices. The TX FIFO in a PRX may be filled up and blocked if all pending payloads are addressed to the pipe where the link to the PTX is lost. In this case, the MCU should flush the TX FIFO by using the FLUSH_TX command.

The TX FIFO may be accessed using three different commands: W_TX_PLOAD, W_ACK_PLOAD, and W_TX_PLOAD_NOACK. All three commands access the same TX FIFO. The description of the commands is detailed in the SPI Command section. The RX FIFO is accessed by the command R_RX_PLOAD, and it may be accessed in both PTX and PRX mode. The payload width of the top slot in RX FIFO is read by the command R_RX_PL_WID.

The statuses of the TX FIFO and RX FIFO are in the STATUS_FIFO register. The device may also be configured to read out the STATUS_FIFO register during every command by adjusting the STAT_SETUP setting in FEATURE register.
The device may retransmit its last transmitted payload by the command REUSE_TX_PL and pulsing the **CE** pin to trigger transmission. Payload reuse will remain active until W_TX_PLOAD or FLUSH_TX command is executed.

5.2 INTERRUPT

TRW-24L01's pin 8 is an active-low interrupt pin, used to inform host MCU of various events. Interrupt is activated when the TX_DS, RX_DR, or MAX_RT in the STATUS register is set high. The IRQ pin is reset when the host writes "1" to the IRQ source bit in the STATUS register. In the CONFIG register, there are three mask bits, which may be used to set which event triggers the IRQ pin. By default all IRQ sources are enabled.

Please note that the 3-bit pipe information in the STATUS register is updated during the **IRQ** pin transition. The pipe information is unreliable if the STATUS register is read during the **IRQ** pin high-to-low transition.

5.3 STAR CONNECTION

TRW-24L01 may be configured as a PRX receiving from up to 6 PTX devices, forming a star network. Once configured, the connections are presented as different data pipes to the PRX host.
The following settings are common to all data pipes:

- CRC on/off (always enabled when using auto-ACK or dynamic payload)
- CRC setting (1 or 2 bytes)
- RX address width
- Frequency channel
- Air data rate

Data pipes are enabled with the EN_RXADDR register. By default data pipe 0 and 1 are enabled. Data pipe addresses are configured in the RX_ADDR_PX register, where “X” is from 0 to 5. Each data pipe should have a unique address. Data pipe 0 has a unique address. Addresses of data pipes 1 to 5 differ only by the LSByte.

During a star connection, since the PRX device will be transmitting ACK packets to different PTX devices, to identify the correct destination, the PRX device uses the RX address of the particular pipe as the packet address when sending ACK packets. Therefore for the PTX devices, their RX address needs to be set the same as their TX address. Furthermore, since all data pipes operate at the same channel frequency, only one data pipe should be active at anytime. When multiple PTXs are transmitting to a PRX, the ARD may be set at different values so that collisions happen only once.

5.4 SPI COMMAND

TRW-24L01 is controlled by a standard SPI interface. All commands must be initiated by a high to low transition on pin **CSN**.

The status of the chip is shifted out on the **MISO** pin simultaneously as the SPI command word is serially fed into the **MOSI** pin. Typically the status output is the STATUS register bits, but it can be configured to report RX status or FIFO status. The output of the MISO pin is set by the STAT_SETUP in the FEATURE register.

The SPI command format consists of an 8-bit command word (from MSB to LSB) followed by the data in bytes. Data bytes are fed from LSByte to MSByte, and start with the MSBit in each byte first.

The R_REG and W_REG commands operate on single or multi-byte registers. When accessing multi-byte registers, writing of bytes may be terminated before all bytes are written, leaving unwritten MSByte(s) unchanged.

Note: The 3 bit pipe information in the STATUS register is updated when **IRQ** pin changes from high to low. Therefore, the pipe information is unreliable if the STATUS register is read during an IRQ transition.

Table 1: SPI Commands

Command name	Command word (binary)	Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode

			Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_ACK_PAYLOAD • W_TX_PAYLOAD_NOACK A new ACTIVATE command with the same data deactivates them again. *This is executable in power down or stand by modes only.* The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on MISO. To activate these registers, use the ACTIVATE command followed by data 0x73. Then they can be accessed as any other register in TRW-24L01. Use the same command and data to deactivate the registers again.
R_RX_PL_WIDa	0110 0000		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOADa	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NOACKa	1011 000	1 to 32 LSByte first	Used in TX mode. Disables AUTOACK on this specific packet.

NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

5.5 SPI TIMING

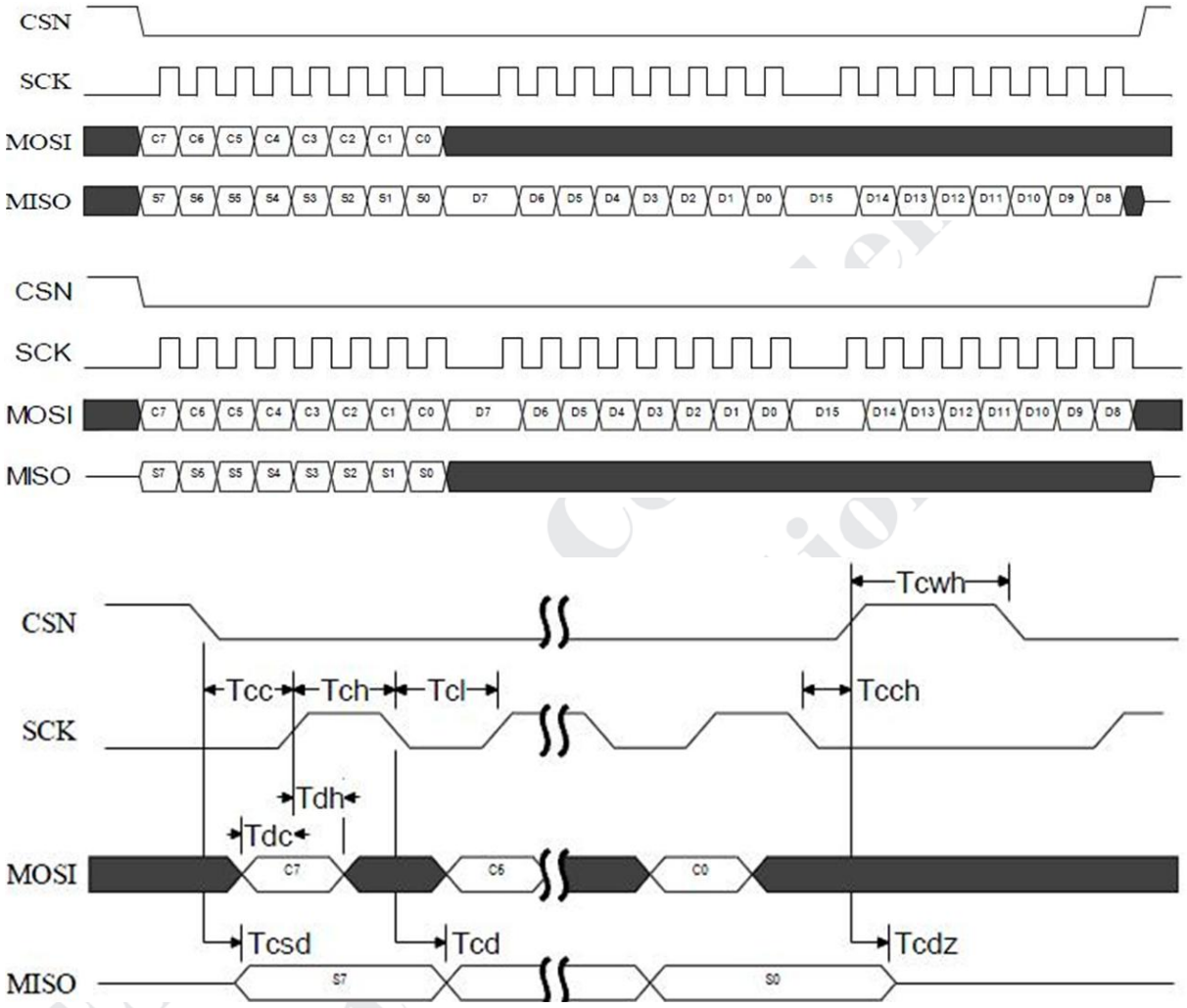


Table 2: SPI Timing

Symbol	Parameters	Minimum	Maximum	Units
Tdc	Data to SCK setup	3		ns
Tdh	SCK to data hold	3		ns
Tcsd	CSN to data valid		38	ns
Tcd	SCK to data valid		55	ns
Tcl	SCK low time	40		ns
Tch	SCK high time	40		ns
Fsck	SCK frequency	0	10	MHz
Tr/Tf	SCK rise & fall time		100	ns
Tcc	CSN to SCK setup	3		ns
Tcch	SCK to CSN hold	3		ns
Tcwh	CSN inactive time	50		ns
Tcdz	CSN to output high Z		38	ns

5.6 MISO STATUS READOUT

By default the MISO will readout the STATUS register during every SPI command input. A feature of TRW-24L01 is that the MISO readout may be set to “RX” focused readout or “FIFO” readout. The MISO readout is set by STAT_SETUP in the FEATURE register. When the register is set to RX readout mode, the positions of MAX_RT and TX_FULL are replaced by RSSI2 and RSSI1. In FIFO readout mode, MISO will read out STATUS_FIFO instead of the STATUS register.

6 REGISTER MAP TABLE

Addresses 0x19, 0x1A, 0x1B, and 0x1F are reserved for test purposes and performance tuning. Altering them to values other than their POR values may result in chip malfunction.

Reserved bits that are labeled “Unused” do not have any function. Reserved bits that are labeled “Only ‘0’ allowed” are not to be changed. Modifications to such reserved bits may result in chip malfunction.

Address (hex)	Name	Bit	Reset value	Type	Description
00	CFG_TOP				Top-level configuration
	Reserved	7	0	R/W	Must be 0 for normal operation
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR; 1: interrupt not reflected on IRQ pin; 0: reflect RX_DR as active low interrupt on IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS; 1: interrupt not reflected on IRQ pin; 0: reflect TX_DS as active low interrupt on IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT; 1: interrupt not reflected on IRQ pin; 0: reflect MAX_RT as active low interrupt on IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if any of the bits in EN_AA is high
	CRCC	2	0	R/W	CRC scheme 0: 1 byte, 1: 2 bytes
	PWR_ON	1	0	R/W	1: power-up, 0, power-down
	RX_ON	0	0	R/W	1: PRX, 0: PTX
01	EN_AA				Auto-acknowledgement settings
	Reserved	7:6	0	R/W	Unused
	ENAA_P5	5	1	R/W	Enable AA on data pipe 5

	ENAA_P4	4	1	R/W	Enable AA on data pipe 4
	ENAA_P3	3	1	R/W	Enable AA on data pipe 3
	ENAA_P2	2	1	R/W	Enable AA on data pipe 2
	ENAA_P1	1	1	R/W	Enable AA on data pipe 1
	ENAA_P0	0	1	R/W	Enable AA on data pipe 0
02	EN_RXADDR				Enable RX addresses
	Reserved	7:6	0	R/W	Unused
	ENRX_P5	5	1	R/W	Enable data pipe 5
	ENRX_P4	4	1	R/W	Enable data pipe 4
	ENRX_P3	3	1	R/W	Enable data pipe 3
	ENRX_P2	2	1	R/W	Enable data pipe 2
	ENRX_P1	1	1	R/W	Enable data pipe 1
	ENRX_P0	0	1	R/W	Enable data pipe 0
03	SETUP_AW				Address width & timing setup
	Reserved	7:4	0	R/W	Unused
	Reserved	3:2	11	R/W	Reserved setting, must be set to 11
	Reserved	1:0	11	R/W	Reserved setting, must be set to 11
04	SETUP_RETR				Automatic retransmission setup
	ARD[3:0]	7:4	0000	R/W	Automatic retransmission delay 0000: wait 250uS 0001: wait 500uS … 1111: wait 4000uS Delay defined as “”
	ARC[3:0]	3:0	0011	R/W	Auto retransmit count 0000: disabled 0001: up to 1 re-transmit on fail of AA … 1111: up to 15 re-transmits on fail of AA
05	RF_CH				RF channel
	Reserve	7	0	R/W	Unused
	RF_CH[6:0]	6:0	0x02	R/W	Set frequency channel in 1 MHz increment, 0x00 is 2400 MHz
06	SETUP_RF				RF settings

	EN_CW	7	0	R/W	Enable continuous carrier when set high Confirm during chip verification
	EN_PRBS	6	0	R/W	Enable PRBS bit stream when set high; EN_CW also needs to be enabled
	RF_DR_LOW	5	0	R/W	See RF_DR_HIGH
	TX_ATTN	4	0	R/W	TX low-power mode Confirm actual attenuation level
	RF_DR_HIGH	3	0	R/W	[RF_DR_LOW, RF_DR_HIGH] 00: 1Mbps 01: 2Mbps 10: 250kbps 11: reserved
	RF_PWR[1:0]	2:1	01	R/W	Set RF output power in TX mode 00: -18 dBm 01: -12 dBm 10: -6 dBm 11: 0 dBm
	Reserved	0	0	R/W	Unused
07	STATUS				Status (read-out from MISO pin during SPI command word input); MISO output may be adjusted
	Reserved	7	0	R/W	Unused
	RX_DR	6	0	R/W	Data ready RX FIFO interrupt. Asserted when new data arrives at RX FIFO. Write 1 to clear bit
	TX_DS	5	0	R/W	Data sent TX FIFO interrupt. Asserted when packet transmitted. If auto-ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit
	MAX_RT	4	0	R/W	Maximum number of TX retransmit interrupt. Write 1 to clear bit. If MAX_RT is

					asserted it must be cleared to enable further operation
	RX_P_NO[2:0]	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000~101: data pipe number (0~5)
	TX_FULL	0	0	R	0: TX FIFO available 1: TX FIFO full
08	OBSERVE_TX				Transmission observation
	PLOS_CNT[3:0]	7:4	0000	R	Count lost packets. Overflow protected to 15, and stops at maximum value until reset. Counter reset by writing to RF_CH
	ARC_CNT[3:0]	3:0	0000	R	Count retransmitted packets. Counter resets when transmission of a new packet starts
09	RSSI				TSSI and RSSI indicator/control
	Reserved	7	0	R/W	Must be 0 for normal operation
	Reserve	6	0	R/W	Must be 0 for normal operation
	Reserved	5	0	R/W	Must be 0 for normal operation
	EN_RSSI	4	0	R/W	Enable RSSI
	Reserved	3	0	R	Reserved register readout
	Reserved	2	0	R	Reserved register readout
	RSSI2	1	0	R	RSSI indicator at threshold 2
	RSSI1	0	0	R	RSSI indicator at threshold 1
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	RX address data pipe 0. 5 bytes maximum. LSB byte written first. Number of bytes used set by SETUP_AW.
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	RX address data pipe 1. 5 bytes maximum. LSB byte written first. Number of bytes used set by SETUP_AW.
0C	RX_ADDR_P2	7:0	0xc3	R/W	RX address data pipe 2. Only LSB are set, MSB

					bytes use RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xc4	R/W	RX address data pipe 3. Only LSB are set, MSB bytes use RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xc5	R/W	RX address data pipe 4. Only LSB are set, MSB bytes use RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xc6	R/W	RX address data pipe 5. Only LSB are set, MSB bytes use RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7 E7E7	R/W	TX address. Used for PTX only. Set RX_ADDR_P0 equal to this address to handle auto acknowledgement
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Unused
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32). 0: pipe not used
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Unused
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32). 0: pipe not used
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Unused
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32). 0: pipe not used
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Unused
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32). 0: pipe not used
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Unused
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX

					payload in data pipe 4 (1 to 32). 0: pipe not used
16	RX_PW_P5				
	Reserved	7:6	00	R/W	Unused
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32). 0: pipe not used
17	STATUS_FIFO				
	Reserved	7	0	R/W	Unused
	TX_REUSE	6	0	R	Used for a PTX device Pulse the rfce high for at least 10μs to Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX *rewrite
	TX_FULL	5	0	R	1: TX FIFO full 0: available slots in TX FIFO
	TX_EMPTY	4	1	R	1: TX FIFO empty 0: data in TX FIFO
	Reserved	3:2	0	R	Reserved register readout
	RX_FULL	1	0	R	1: RX FIFO full 0: available slots in RX FIFO
	RX_EMPTY	0	1	R	1: RX FIFO empty 0: RX FIFO full
18	RSSIREC				RSSI recorder feature
	Reserved	31:26	111	W	Reserved
	Reserved	25:22	0110	R	Reserved
	RX_VREF2_SEL[2:0]	21:19	000	W	RX RSSI VREF2 setting 000: -59 dBm, +4dB/step 111: out of range
	RX_VFEF1_SEL[2:0]	18:16	000	W	RX RSSI VREF1 setting 000:-69 dBm, +4dB/step
	RSSIREC2[7:0]	15:8	01110010	R	RSSI2 recorder, MSB is most recent recording, any

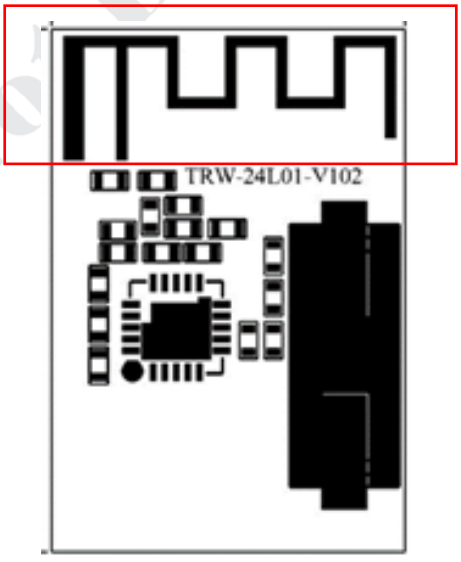
					write command on this register will flush RSSI setting; when RX_ON=0, PWR_ON=0 & CE=0, register will read chip ID
	RSSIREC1[7:0]	7:0	01000001	R	RSSI1 recorder, MSB is most recent recording, any write command on this register will flush RSSI setting; when RX_ON=0, PWR_ON=0 & CE=0, register will read chip ID
1C	DYNPD				Dynamic payload length
	Reserved	7:6	00	R/W	Unused
	DPL_P5	5	0	R/W	Set 1 to enable dynamic payload length data pipe 5 (requires EN_DPL & ENAA_P5)
	DPL_P4	4	0	R/W	Set 1 to enable dynamic payload length data pipe 4 (requires EN_DPL & ENAA_P4)
	DPL_P3	3	0	R/W	Set 1 to enable dynamic payload length data pipe 3 (requires EN_DPL & ENAA_P3)
	DPL_P2	2	0	R/W	Set 1 to enable dynamic payload length data pipe 2 (requires EN_DPL & ENAA_P2)
	DPL_P1	1	0	R/W	Set 1 to enable dynamic payload length data pipe 1 (requires EN_DPL & ENAA_P1)
	DPL_P0	0	0	R/W	Set 1 to enable dynamic payload length data pipe 0 (requires EN_DPL & ENAA_P0)
1D	FEATURE				Features
	STAT_SETUP[1:0]	7:6	00	R/W	Adjust the output of MISO during command input 00: default, MISO output is

					STATUS 01: RX readout mode, the MISO output MAX_RT and TX_FULL bit is replaced by RSSI2 and RSSI1 readout 10: FIFO readout mode, MISO output is STATUS_FIFO 11: unused, same as 00
	Reserved	5:3	000	R/W	Unused
	EN_DPL	2	0	R/W	Set 1 enables dynamic payload length
	EN_ACK_PAY	1	0	R/W	Set 1 enables payload on ACK
	EN_DYN_ACK	0	0	R/W	Set 1 enables the W_TX_PAYLOAD_NOACK command
1F	RESERVED				Reserved register
	Reserved	7:0	0	R/W	8'h00: default settings

7 Reference schematics

Attached reference schematics give an example how to have TRW-24L01 module to work with micro-controller, it might be 8051, chips of microchip or any embedded SOC, to communicate with host through RS-232 interface. U4 is RS-232 transceiver chip which converts signals level.

Remark：Antenna wiring should not be positioned above or under the ground layer, power layer and the other wirings.



Size View