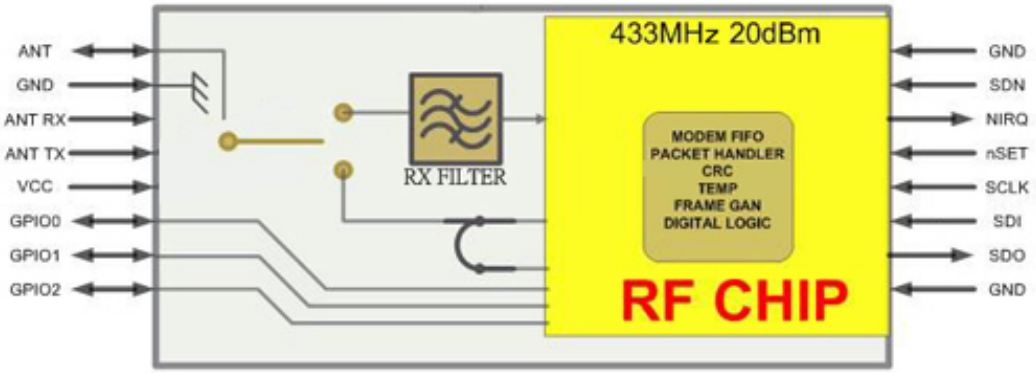
433MHz ISM Transceiver Module

TRW - 4432 - 433

Function Block Diagram



Version History

Version	Date	Changes
V1.00	September 26, 2013	1st. Edition
V1.00	November 19, 2013	1st. Edition

Key Features

- Worldwide 433 ISM band operation
- 0.123 to 256KBPs on air datarates
- Ultra low power operation
- Output power range +20 dBm Max
- 18.5 mA receive, 85 mA @ +20 dBm transmit
- Digital RSSI
- FSK, GFSK, and OOK modulation
- Low cost
- 1.8 to 3.6V supply range
- Temperature sensor and 8-bit ADC
- Automatic packet handling
- Auto packet transaction handling
- TX and RX 64 byte FIFOs
- On-chip crystal tuning

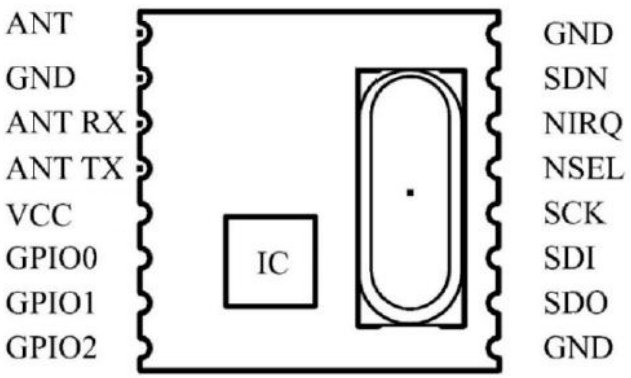
Applications

- Wireless PC Peripherals
- Sensor networks
- Toys
- Sports watches and sensors
- Home and commercial automation
- Active RFID
- Home security & alarm
- Advanced Media center remote controls
- Game controllers
- RF remote controls for consumer electronics
- Ultra low power sensor networks
- Asset tracking systems

Product Description

TRW-4432-433 是完全集成的高功率無線模組，高性能收發器設計，可在非常低的功耗下達到最大效率值。該模組主要用於 ISM（工業，科學和醫學）和 SRD（短距離設備），頻率波段 420MHz~450MHz，內制 PA，輸出達+19dBm。可由 SPI 介面調整功率，彈性控制輸出功率，通過 SPI 接口控制，既可控制輸出及接收資料，且可讀出 RF IC 之溫度，以便及時了解本模組是否在工作溫度範圍內。

Pin Assignments



Pin Function

Pin	Name	I/O	Description
1	Antenna	Input/output	Antenna
2	GND	GND	Ground
3	ANT RX	Input	Controlled antenna switch, IF Receiver MODE IS High Voltage
4	ANT TX	Input	Controlled antenna switch, IF Transmitter MODE IS High Voltage
5	VCC	Input	+1.8V to +3.6 V Supply Voltage Input to Internal Regulators
6	GPIO0	Digital I/O	General Purpose Digital I/O that may be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc. See the SPI GPIO Configuration Registers, Address 0Bh, 0Ch, and 0Dh for more information.
7	GPIO1	Digital I/O	
8	GPIO2	Digital I/O	
9	GND	GND	ground.
10	SDO	Digital Output	Provides a serial read back function of the internal control registers.
11	SDI	Digital Input	This pin provides the serial data stream for the 4-line
12	SCLK	Digital Input	Serial Clock Input. digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the RF CHIP on positive edge transitions
13	nSEL	Digital Input	Serial Interface Select input. 0– VDD V digital input. This pin provides the Select/Enable function for the 4- line serial data bus. The signal is also used to signify burst read/write mode
14	NIRQ	Digital Output	General Microcontroller Interrupt Status output. When the Si4430/31/32 exhibits anyone of the

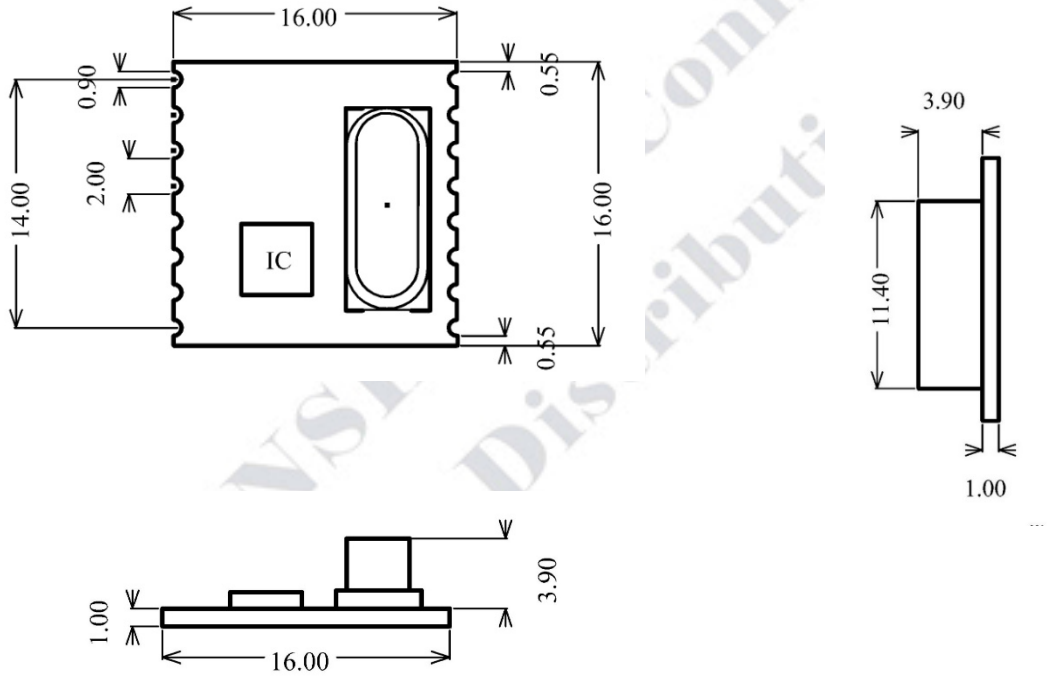
			Interrupt Events the nIRQ pin will be set low=0. Please see the Control Logic registers section for more information on the Interrupt Events. The Microcontroller can then determine the state of the interrupt by reading a corresponding SPI Interrupt Status Registers, Address 03h and 04h. No external resistor pull-up is required, but it may be desirable if multiple interrupt lines are connected
15	SDN	Digital Input	Shutdown input pin. 0–VDD V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN =1 the chip will be completely shut down and the contents of the registers will be lost.
16	GND	GND	Ground

1 Hardware Specification

1.1 Specification

Conditions: VDD =VCC= 3V, VSS = 0V, TA = 25ºC

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Supply Voltage Range	Power		1.8	3	3.6V	V
Power Down	Power	Power Down		15		nA
RX Mode Current	Receiver	1KBPS		18.5		mA
TX Mode Current	Transmitter	20dBm			85	mA
RX Sensitivity	Receiver	512bps 433MHz	-121dBm			dBm



Support

本模組 TRW-4432-433 內置天線開關，在發射或接收時必須控制 ANT TX 及 ANT RX 這兩個 PIN，可透過 MCU 控制或由 GPIO 0、GPIO 1、GPIO2 控制。

例: GPIO-0 接至 ANT TX PIN、GPIO-1 接至 ANT RX PIN，在接收模式時須宣告 GIPIO-0 為 LO，GPIO-1 為 HI；在發射模式時需宣告 GPIO-0 為 HI，GPIO-1 為 LO。

	GPIO-0	GPIO-1	NS
接收	LO	HI	
發射	HI	LO